

FIG. 1

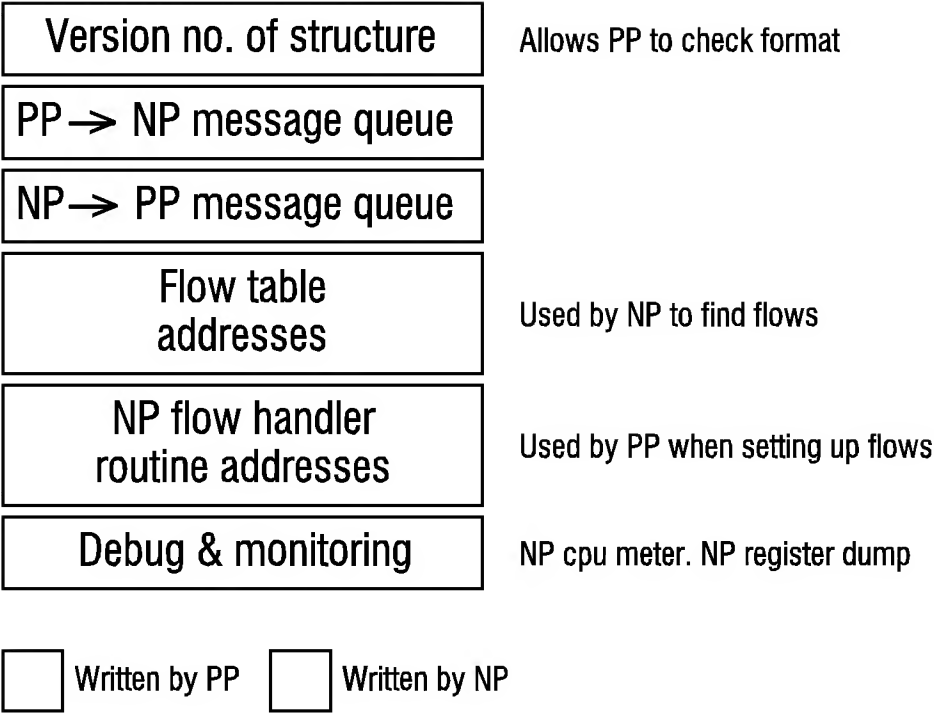
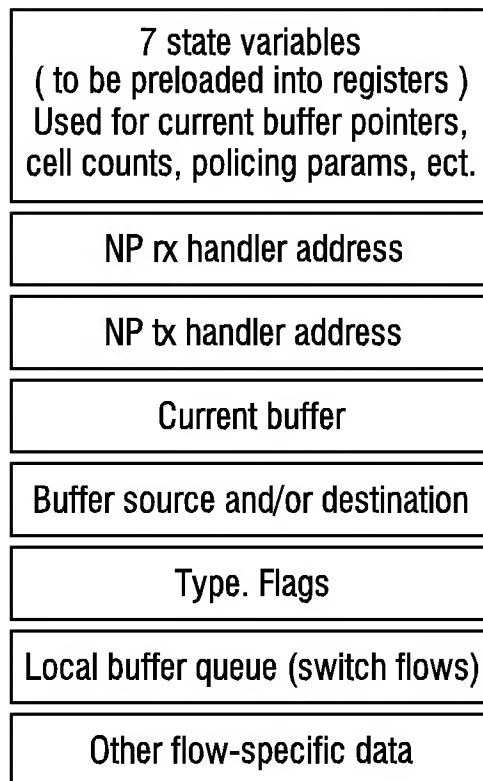


FIG. 4



First part has a similar format in all follows.

A flow is invoked by a single instruction:

- loads 8 or 9 registers
- jumps to handler routine

FIG. 5

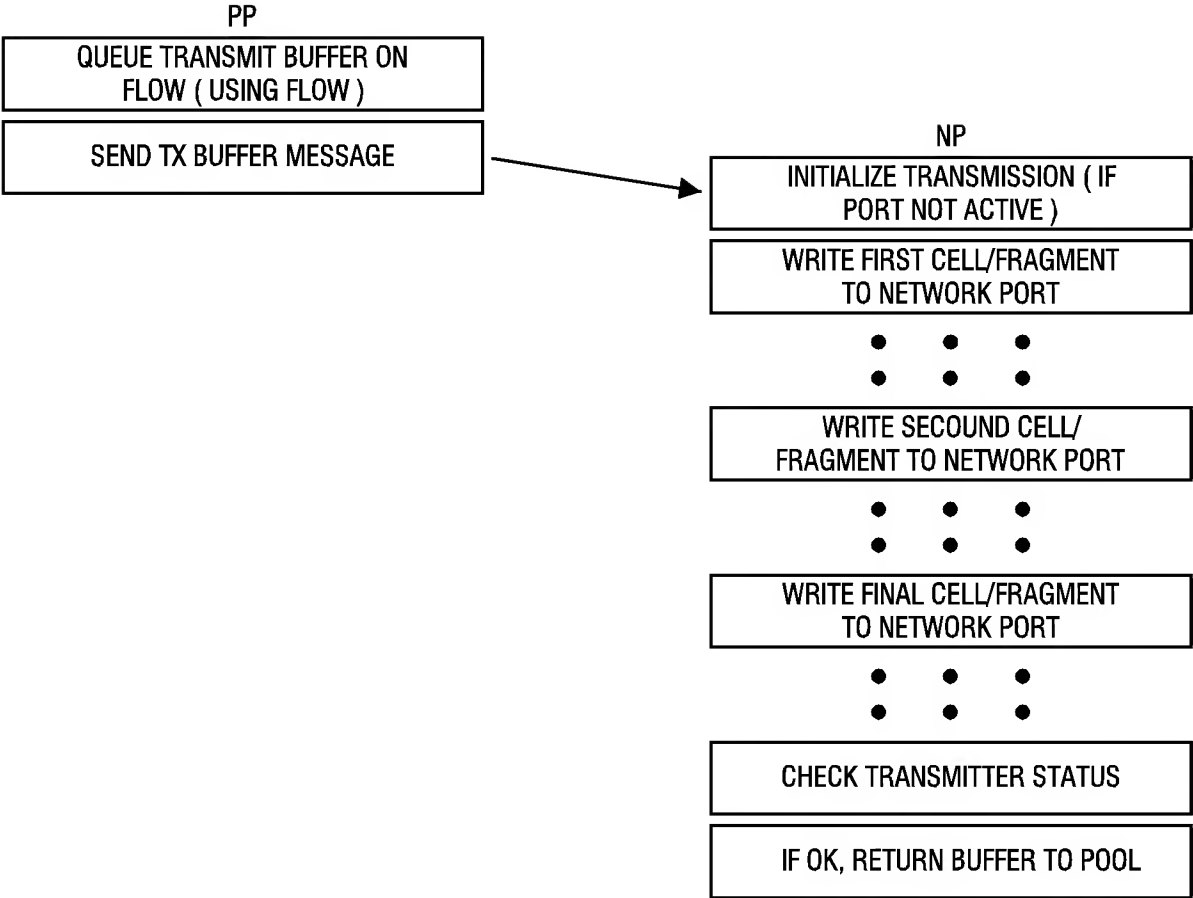


FIG. 6

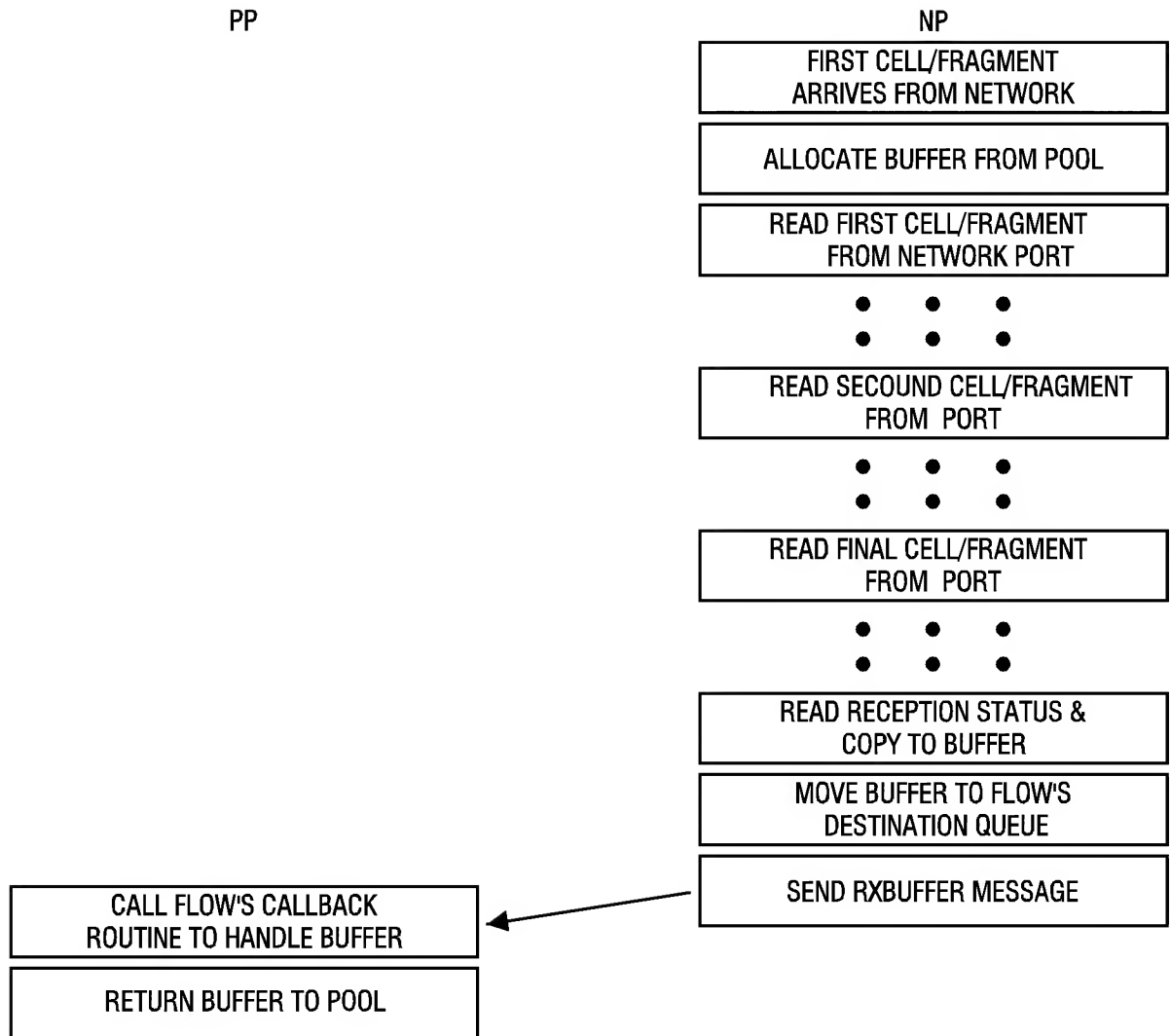


FIG. 7

Replacement Sheet

OCTETS field in TX_ALIGN field in	Least significant 2 bite of DMA adress	Keep _ALIGN flag	TEXT_ALIGN register word at start	Next word from memory	TEXT_ALIGN register word after first memory cycle	Word written to FIFO
XX	00	0	XXXX . XXXX	pqrs . vwyz	XXXX . XX00	pqrs . vwyz
XX	01	0	XXXX . XXXX	pqrs . vwyz	pqrs . vw01	No write
XX	10	0	XXXX . XXXX	pqrs . XXXX	pqrs . vw02	No write
XX	11	0	XXXX . XXXX	pqXX . XXXX	pqXX . vw03	No write
00	00	1	XXXX . XX00	pqrs . vwyz	XXXX . XX00	pqrs . vwyz
00	01	1	XXXX . XX00	pqrs . vwXX	pqrs . vw01	No write
00	10	1	XXXX . XX00	pqrs . XXXX	pqrs . vw02	No write
00	11	1	XXXX . XX00	pqXX . XXXX	pqXX . vw03	No write
01	00	1	ghij . klo1	pqrs . vwyz	pqrs . vw01	yagh . ijk1
01	01	1	ghij . klo1	pqrs . vwXX	pqrs . vw02	vwgh . ijk1
01	10	1	ghij . klo1	pqrs . XXXX	pqXX . vw03	ragh . ijk1
01	11	1	ghij . klo1	pqXX . XXXX	XXXX . XX00	pqgh . ijk1
10	00	1	ghij . XX02	pqrs . vwyz	pqrs . vw02	vwyz . ghij
10	01	1	ghij . XX02	pqrs . vwXX	pqXX . vw03	rsvw . ghij
10	10	1	ghij . XX02	pqrs . XXXX	XXXX . XX00	pqrs . ghij
10	11	1	ghij . XX02	pqXX . XXXX	pqgh . ij01	No write
11	00	1	ghXX . XX03	pqrs . vwyz	pqXX . vw03	rsvw . yzgh
11	01	1	ghXX . XX03	pqrs . vwXX	XXXX . XX00	pqrs . vwgh
11	10	1	ghXX . XX03	pqrs . XXXX	pqrs . gh01	No write
11	11	1	ghXX . XX03	pqXX . XXXX	pqgh . XX02	No write

FIG. 10

OCTETS field in TX_ALIGN register	TEXT_ALIGN register word at start	word writing to FIFO register	FIFO register written	TEXT_ALIGN after FIFO register write	Word written to FIFO
00	XXXX . XX00	pqrs . vwyz	TX . FIFO0	XXXX . XX00	pqrs . vwyz
00	XXXX . XX00	XXrs . vwyz	TX . FIFO1	rsvw . yz01	No write
00	XXXX . XX00	XXXX . vwyz	TX . FIFO2	vwzy . XX02	No write
00	XXXX . XX00	XXXX . XXyz	TX . FIFO3	yzXX . XX03	No write
01	ghij . klo1	pqrs . vwyz	TX . FIFO0	pqrs . vw01	yzgh . ijk1
01	ghij . klo1	XXrs . vwyz	TX . FIFO1	rsvw . XX02	yzgh . ijk1
01	ghij . klo1	XXXX . vwyz	TX . FIFO2	vwXX . XX03	yzgh . ijk1
01	ghij . klo1	XXXX . XXyz	TX . FIFO3	XXXX . XX00	yzgh . ijk1
10	ghij . XX02	pqrs . vwyz	TX . FIFO0	pqrs . XX02	vwyz . ijk1
10	ghij . XX02	XXrs . vwyz	TX . FIFO1	rsXX . XX03	vwyz . ijk1
10	ghij . XX02	XXXX . vwyz	TX . FIFO2	XXXX . XX00	vwyz . ijk1
10	ghij . XX02	XXXX . XXyz	TX . FIFO3	pqgh . ij01	No write
11	ghXX . XX03	pqrs . vwyz	TX . FIFO0	pqXX . XX03	rsvw . yzgh
11	ghXX . XX03	XXrs . vwyz	TX . FIFO1	XXXX . XX00	rsvw . yxgh
11	ghXX . XX03	XXXX . vwyz	TX . FIFO2	vwyz . gh01	No write
11	ghXX . XX03	XXXX . XXyz	TX . FIFO3	yzgh . XX02	No write

FIG. 11

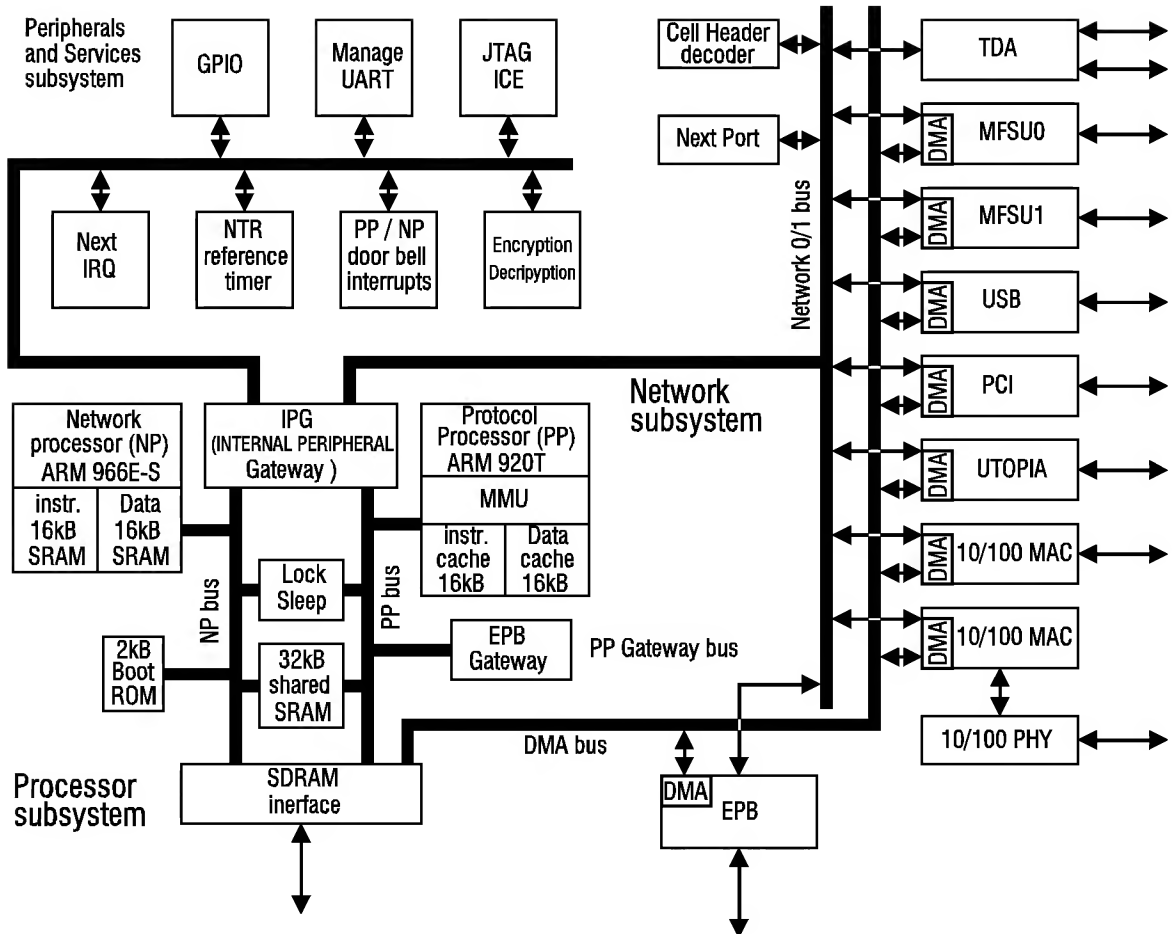


FIG. 12

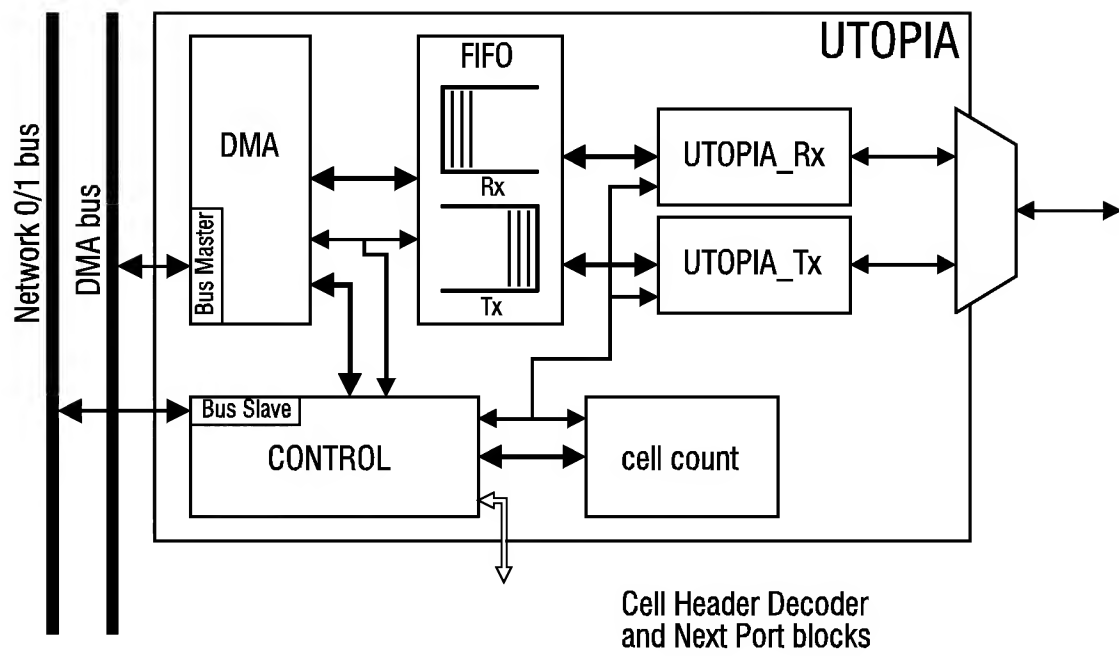


FIG. 13

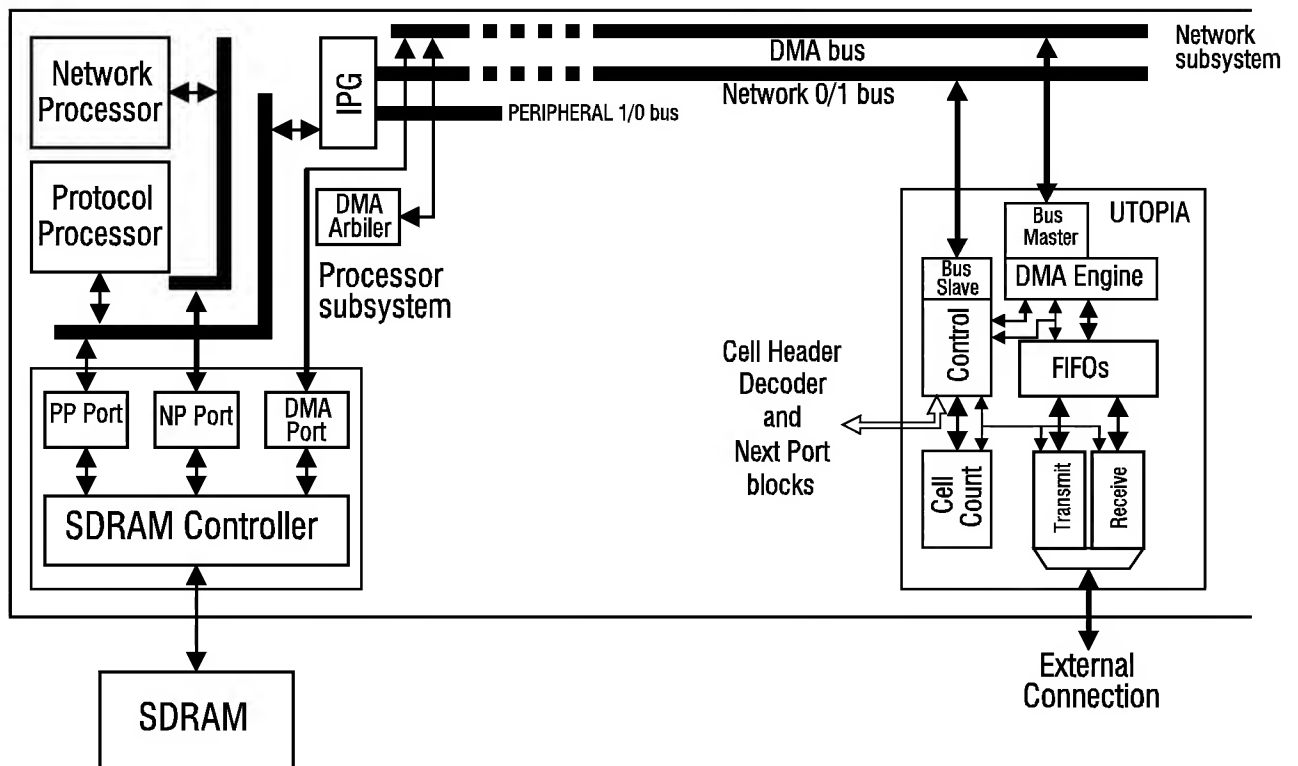


FIG. 14

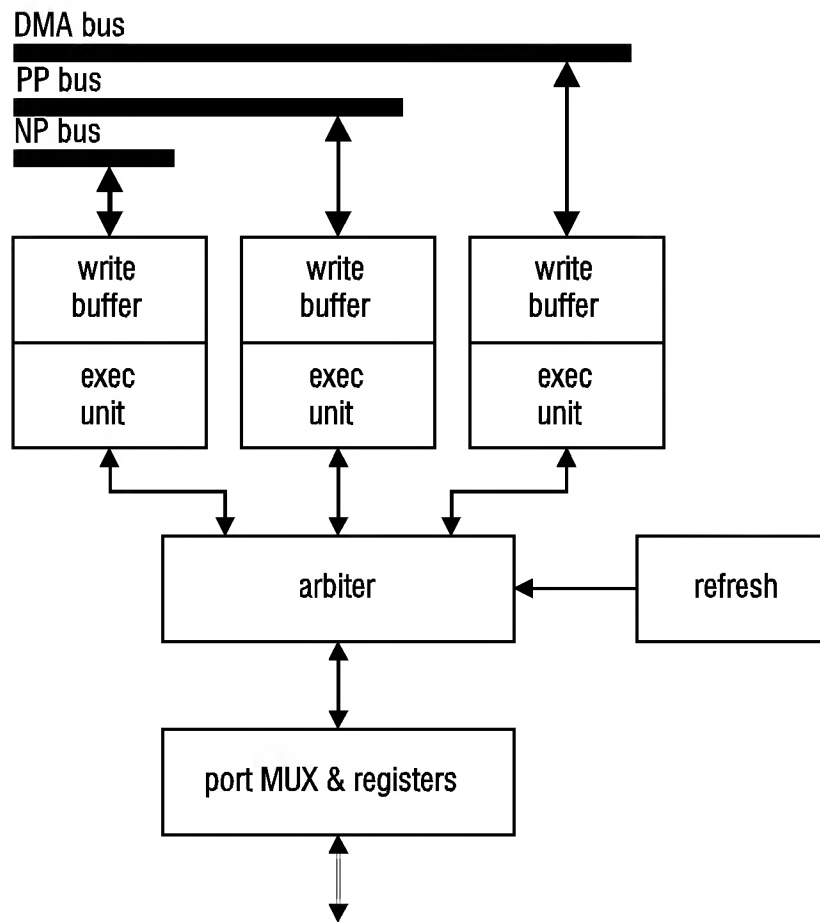


FIG. 15

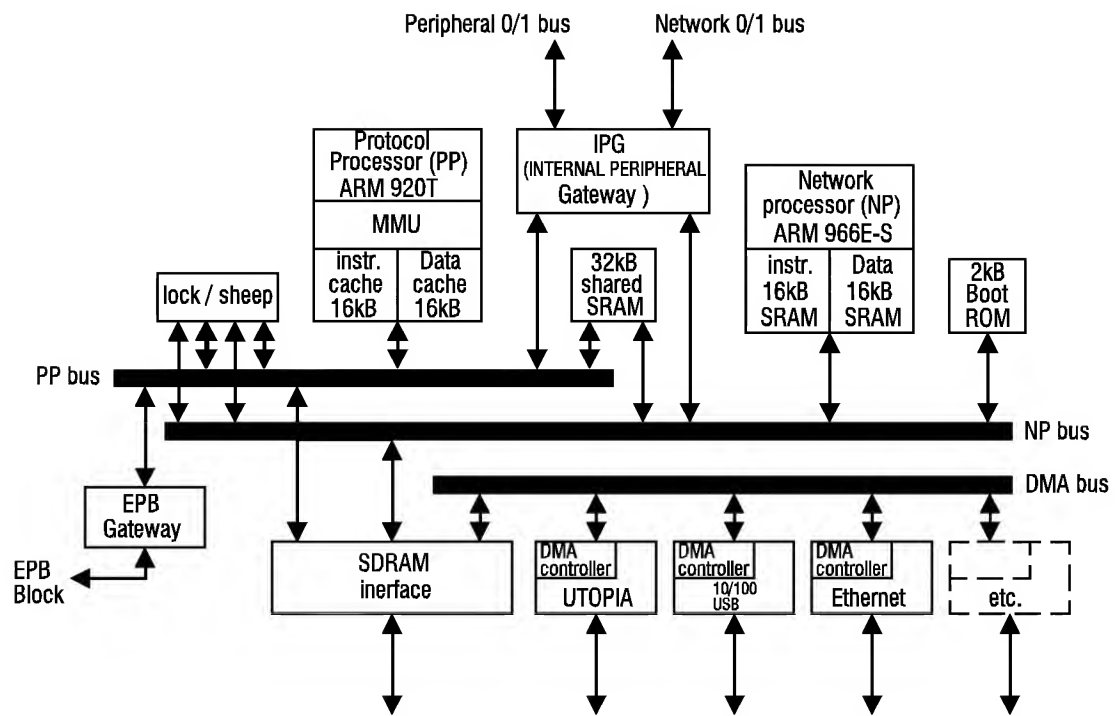


FIG. 16

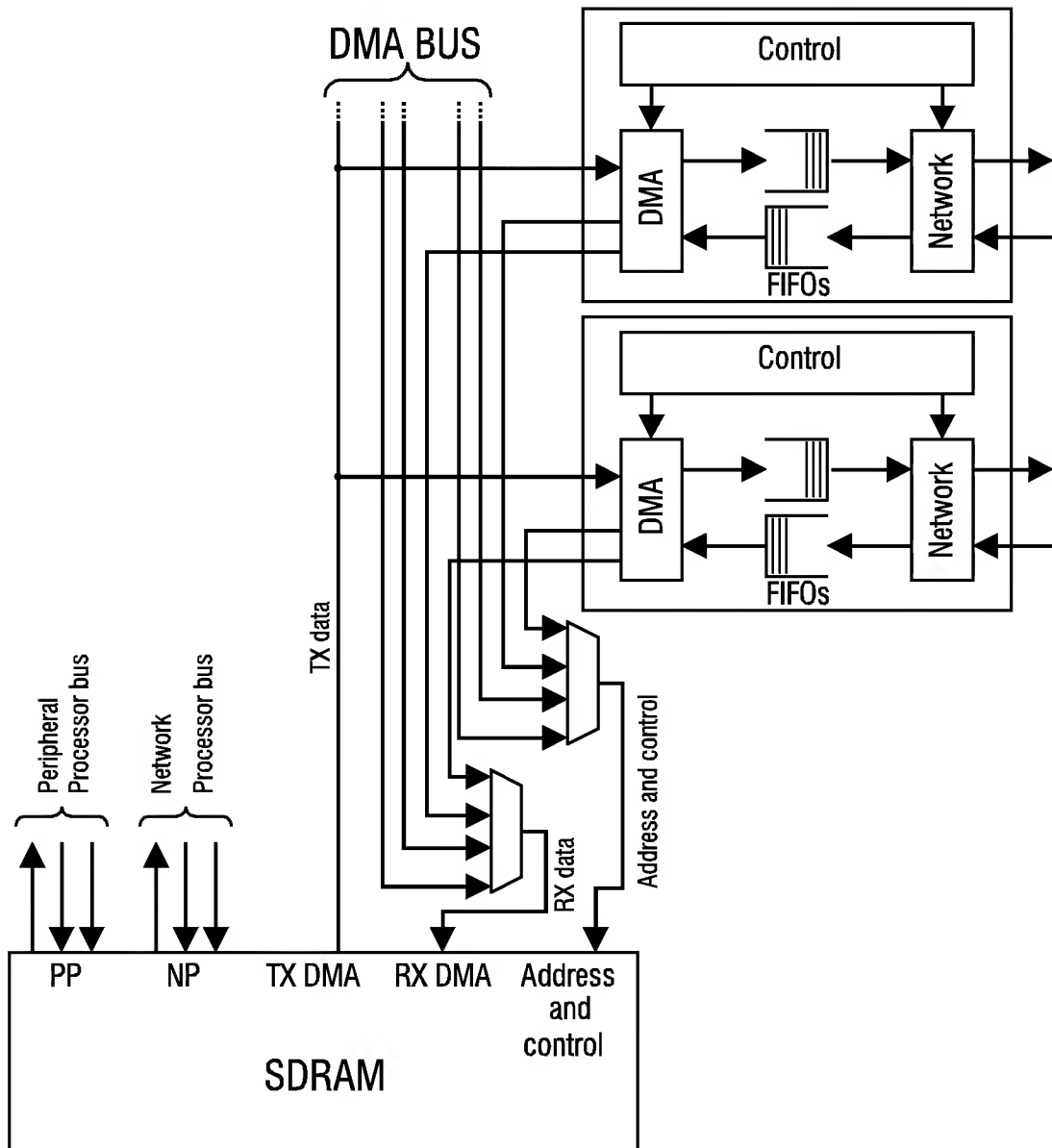


FIG. 17